**In the Specification**

Please replace the paragraph beginning on page 2, line 21 with the following amended paragraph:

Figure 1 shows, for example, a graph representing the current flowing [(I[μA]), (0-70 μA)] in a multilevel memory cell storing two bits and the reference currents defining reference intervals used for reading the contents of the memory cell.

Please replace the paragraph beginning on page 8, line 12 with the following amended paragraph:

The reading of multilevel memory cells is then strongly influenced by the precision and by the repeatability of the reading voltage supplied to the gate terminals of the memory cells during successive reading operations, the precision and repeatability depending to a marked extent upon the presence of ripple on the reading voltage ($V_{READ}$), the variation of the operating temperature of the memory device, the variation of the supply voltage supplied from outside the memory device, and any excessively close memory accesses.

Finally, reading of multilevel memory cells is also influenced by the gain spread of the memory cells due to process spreads, by the widening of the distributions of the drain currents $I_D$ caused by the gain variation of the multilevel memory cells, which is in turn caused by variations in the operating temperature ($T_1$ $T_2$) of the memory device, as shown in Figure 9, and by the compression of the distributions of the drain currents $I_D$ of the multilevel memory cells caused by minimum-gain memory cells, as highlighted in Figure 10.

Please replace the paragraph beginning on page 16, line 16 with the following amended paragraph:

It will thus immediately be clear to the reader skilled in the art how what is illustrated in Figure 15 with regard to the reading of memory cells that store two bits 10 each can be extended

to the reading of memory cells that store *n* bits. In this case, in fact, it will be necessary to use $2^{n-1}$ reference memory cells 7 and $2^{n-1}$ sense amplifiers 8 for generating the reference-latch signals.

Please replace the paragraph beginning on page 17, line 7 with the following amended paragraph:

As is evident also from Figure 14, the contents of the array memory cell 3 being read are simply the two bits ("11", "10", "01", and "00") present on the bus 10 when the cell-latch signal $LATCH_{CELL}$ switches, so that the switching of the cell-latch signal $LATCH_{CELL}$ may be used for storing the contents of the bus 10 at that time, and these contents constitute the datum stored in the array memory cell being read.